Progressive Breakdown in High-Voltage GaN MIS-HEMTs

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***Abstract*—We have investigated the time-dependent dielectric breakdown (TDDB) characteristics of high-voltage AlGaN/GaN Metal-Insulator-Semiconductor High Electron Mobility Transistors (MIS-HEMTs). We focus in particular on the phenomenon known as progressive breakdown (PBD), marked by an onset of noise in the gate current I_G during forward gate bias stress. We observe classic PBD behavior characterized by a rapid increase of I_G noise during stress that takes place soon before hard breakdown (HBD). The onset of PBD also marks a change in the subthreshold characteristics of the transistor: the gate leakage increases above the measurement noise floor in a step-like fashion, with this additional leakage flowing out the source and/or drain terminals. After PBD, the subthreshold I_G also shows a power law temperature dependence. The capacitance-voltage characteristics measured both before and after PBD confirm that device degradation does not occur at the AlGaN/GaN interface. All results are consistent with observations in silicon MOSFETs that support the percolation model of defects behind PBD and HBD. This gives hope that proper physical models suitable for lifetime estimation can be developed for TDDB in GaN MIS-HEMTs.**

***Index Terms*—GaN, MIS-HEMT, TDDB, progressive breakdown, dielectric reliability**

I. Introduction

As the demand for more energy-efficient electronics increases, GaN Field-Effect Transistors (FETs) have emerged as promising candidates for high-voltage power management applications. The AlGaN/GaN metal-insulator-semiconductor high electron mobility transistor (MIS-HEMT) constitutes the prevailing device structure for power switching applications as it offers lower gate leakage than its HEMT counterparts. Though GaN has excellent material properties, there are still many challenges to overcome before GaN transistors are ready for commercial deployment [1]–[3]. Time-dependent dielectric breakdown (TDDB), a catastrophic condition that arises after prolonged high-voltage gate bias stress [4], is a particularly important concern that has not yet received sufficient attention in GaN MIS-HEMTs [5],[6]. Our work focuses on gate dielectric reliability and in particular, in contributing fundamental understanding of the physics behind TDDB of the gate dielectric. Towards this end, we investigate in this paper the behavior of progressive breakdown (PBD) in GaN MIS-HEMTs, which to our knowledge has not been studied before.

There are several challenges involved in carrying out TDDB studies in GaN MIS-HEMTs. First, the gate stack contains multiple layers and several interfaces. This gives rise to a somewhat uncertain electric field distribution. Second, there can be complex dynamics involved after high voltage stress as this can cause electron trapping in the AlGaN barrier [7], in the gate dielectric and at its interface [8], as well as electron accumulation at the AlGaN/dielectric interface that is known to respond rather slowly [8]. These complex dynamics result in a rather unstable and fast changing threshold voltage V_T that complicates TDDB studies in these devices.

In a previous work, we demonstrated an experimental approach that allows us to isolate the different roles of V_T shift, dielectric trapping, interface state generation, and stress-induced leakage current (SILC) under high positive gate voltage stress [6]. Using this methodology, we found that TDDB in GaN MIS-HEMTs exhibits a classic TDDB behavior that is similar in many respects to that of silicon devices.

In this work, we focus on a regime of breakdown known as progressive breakdown, or PBD. As this is a condition that is at times observed very close to the complete breakdown of the gate dielectric (hard breakdown or HBD), studying PBD could provide valuable insight into the hard breakdown physics. We carry out this study using our experimental methodology that allows us to characterize devices during stress experiments in the presence of device instability [6]. We explore the statistical behavior of PBD, and examine the change in the gate current characteristics, as well as its temperature dependence, during the PBD phase. Capacitance-voltage characterization is also used to complete a more well-rounded understanding of the progressive breakdown phenomenon.

II. Experimental Methodology and Breakdown Statistics

The devices studied in this work are industrially prototyped AlGaN/GaN MIS-HEMTs fabricated on a 6-inch wafer. They feature three field plates placed in a stairway fashion along the gate-to-drain gap that results in a breakdown voltage >600 V. All experiments were carried out using an Agilent B1505A Power Device Analyzer equipped with High Power Source Measurement Units (HPSMUs) and a Capacitance Measurement Unit (CMU). The stress of these NFETs is performed under positive gate voltage, $V_{GS,stress}>0$ V, while keeping $V_{DS,stress}=0$ V. This induces a high-density 2DEG at the AlGaN/GaN interface below the gate.

Fig. 1 shows the evolution of the bias gate current, I_G, in a typical constant-voltage TDDB experiment at $V_{GS,stress}=12.6$

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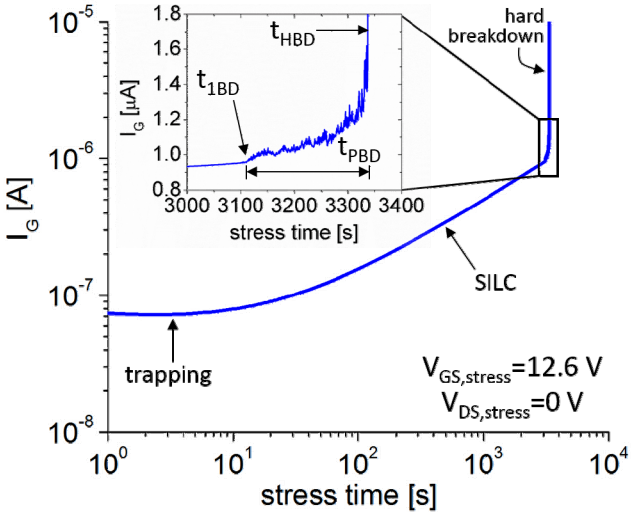

Fig. 1. Gate current as a function of stress time during a constant $V_{GS,stress}$ TDDB experiment. The FET is held at $V_{GS,stress}$=12.6 V until the device breaks down. $V_{DS,stress}$=0 V. The inset shows detail of bias I_G evolution right before hard breakdown (HBD). The clear onset of noise in I_G marks the beginning of progressive breakdown (PBD).

V. The slight decrease of I_G in the initial stages of the experiment is indicative of trapping [9], and the increase of I_G thereafter can be attributed to stress-induced leakage current, SILC [10]. Dielectric hard, i.e. catastrophic, breakdown (HBD) is observed to take place around 3400 s. The inset shows that approaching HBD, I_G becomes noisy, a condition known as progressive breakdown (PBD) [11]. This is distinct from the SILC we see before. While SILC is the increased leakage that results from defects being generated everywhere within the dielectric in accordance with the percolation model [12], PBD reflects the formation of a breakdown path created by these defects within the dielectric [13]. After the onset of PBD, further stress increases the I_G noise until HBD occurs. We denote the time at which gate noise appears as the time-to-first-breakdown, t_{1BD}, the time at which final hard breakdown occurs as t_{HBD}, and the time lapse in between as the length of PBD, or t_{PBD}.

Fig. 2 shows a Weibull plot for time-to-first-breakdown t_{1BD}, and time to HBD, t_{HBD}, of several devices stressed under identical conditions. Well-behaved Weibull statistics are observed with a Weibull slope [14] β of 5.5 and 5.9 for 1BD and HBD, respectively. These values are significantly higher than reports in other GaN MIS-HEMT systems [5], [15]–[17]. The nearly parallel shift in the Weibull distributions of 1BD and HBD suggests a common origin for the two phenomena. Once first breakdown occurs, additional gate stress continues to generate defects at random. Eventually HBD takes place when enough energy is suddenly delivered to the PBD breakdown path so that it becomes nearly ohmic [18]. Thus, from device to device, we expect t_{1BD} and t_{HBD} to be uncorrelated but the overall statistics to be similar. Indeed, if we plot the time-to-first-breakdown t_{1BD} with its corresponding PBD time, t_{PBD}, as shown in Fig. 3 and done in [19], we see that the two are independent of one another.

By itself, the experiment in Fig. 1 yields limited understanding of the physics at play. We can gain greater insight by pausing the gate stress and periodically

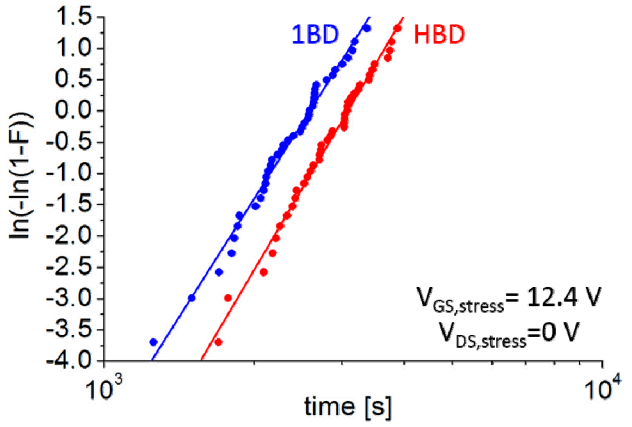

Fig. 2. Weibull plot of t_{1BD} and t_{HBD}. $V_{GS,stress}$=12.4 V, $V_{DS,stress}$=0 V. Nearly parallel statistics for time-to-first-breakdown 1BD and HBD suggest a unified degradation mechanism.

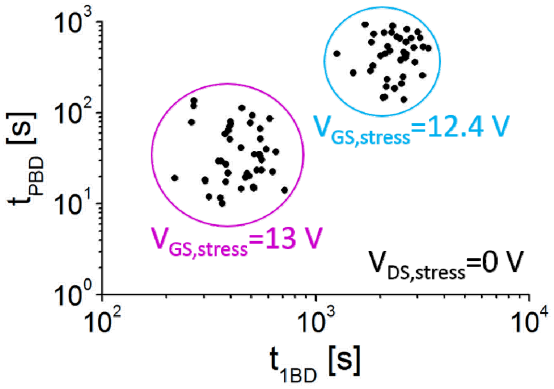

Fig. 3. PBD time vs. time-to-first-breakdown t_{1BD} for samples stressed at $V_{GS,stress}$=12.4 V and $V_{GS,stress}$=13 V. Both sets of data show that t_{1BD} and t_{PBD} are uncorrelated. As $V_{GS,stress}$ increases both t_{1BD} and t_{PBD} decrease as well. $V_{DS,stress}$=0 V.

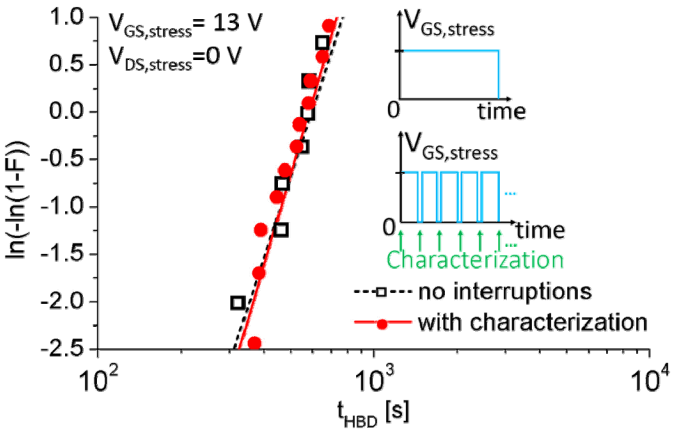

Fig. 4. Weibull plot of time to device hard breakdown (t_{HBD}) for experiments with constant $V_{GS,stress}$ and no pauses for characterization (black symbols, top of inset) and experiments pausing during stress to characterize the device (red symbols, bottom of inset). F is defined as the fraction of devices that have reached breakdown.

characterizing the device by examining its I-V characteristics. This is sketched in the inset of Fig. 4. To confirm that our new scheme has not affected the overall statistics, we carry out TDDB experiments both with a conventional approach

(constant stress, no interruptions), and also under the scheme that includes periodic interruptions to measure the I-V characteristics. The identical statistical results for time to hard breakdown t_{HBD} in the Weibull plot of Fig. 4 for both schemes indicate that the added complexity has not affected the breakdown measurements.

We can further add to our stress-and-measurement methodology by separating the TDDB stress into pre-1BD and post-1BD phases, where the post-1BD phase is the PBD regime. Because the duration of PBD is small compared to the overall stress time, we characterize the device every 5 minutes until 1BD has occurred, after which we characterize the device every 20 s, as shown in the inset of Fig. 5. This figure shows the evolution of bias I_G during a typical interrupted gate stress experiment. The small drop in I_G at the beginning of each stress step can be attributed to minor electron re-trapping that follows electron de-trapping (in the dielectric or in the AlGaN barrier) during the characterization phase. The results from experiments of this kind are discussed next.

III. Subthreshold Characterization

A. *Before First Breakdown*

Fig. 6 shows the current-voltage characteristics at V_{DS}=0.1 V of a device in its virgin state and after various stress times *before* 1BD takes place. Immediately after the application of stress, there is a large positive V_T shift followed by a slower and smaller negative V_T shift as the stress continues. This positive V_T shift has been observed by us [6] and other authors [12]-[13] and is attributed to electron trapping in the oxide. Fig. 6b shows that an immediate increase in the subthreshold swing S of the drain current takes place right after the onset of stress, but shows no trend as the stress continues. This suggests the degradation of S is not linked to the gradual degradation of the dielectric. In 6c we see identical behavior of I_S as we do for I_D, and in the inset observe that I_G remains below the noise floor of our measurement system.

B. *After First Breakdown*

Figs. 7 and 8 show subthreshold I-V characteristics measured every 20 s *after* 1BD has occurred. Fig. 7a shows that beyond 1BD, I_G prominently rises above the noise floor and increases as the stress evolves. I_G seems to increase in sudden jumps, suggesting the discrete formation of defects along the breakdown path during stress. We also see from Fig. 7b that the excess I_G current flows preferentially through the source. Fig. 8 shows that the current through the drain is largely unaffected by the occurrence of PBD. Thus, the breakdown path in the dielectric for this particular device is likely closer to the source. Similar studies in multiple devices

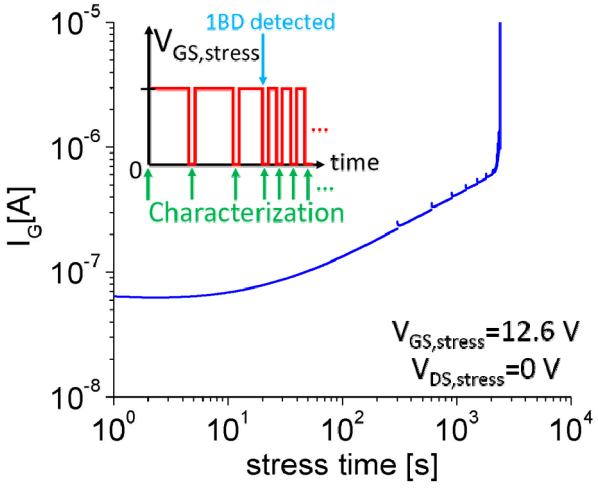

Fig. 5. Gate current as a function of stress time where $V_{GS,stress}$ is paused periodically to measure the I-V characteristics. Characterization is performed every 5 minutes before 1BD and every 20 s after 1BD. $V_{GS,stress}$=12.6 V and $V_{DS,stress}$=0 V.

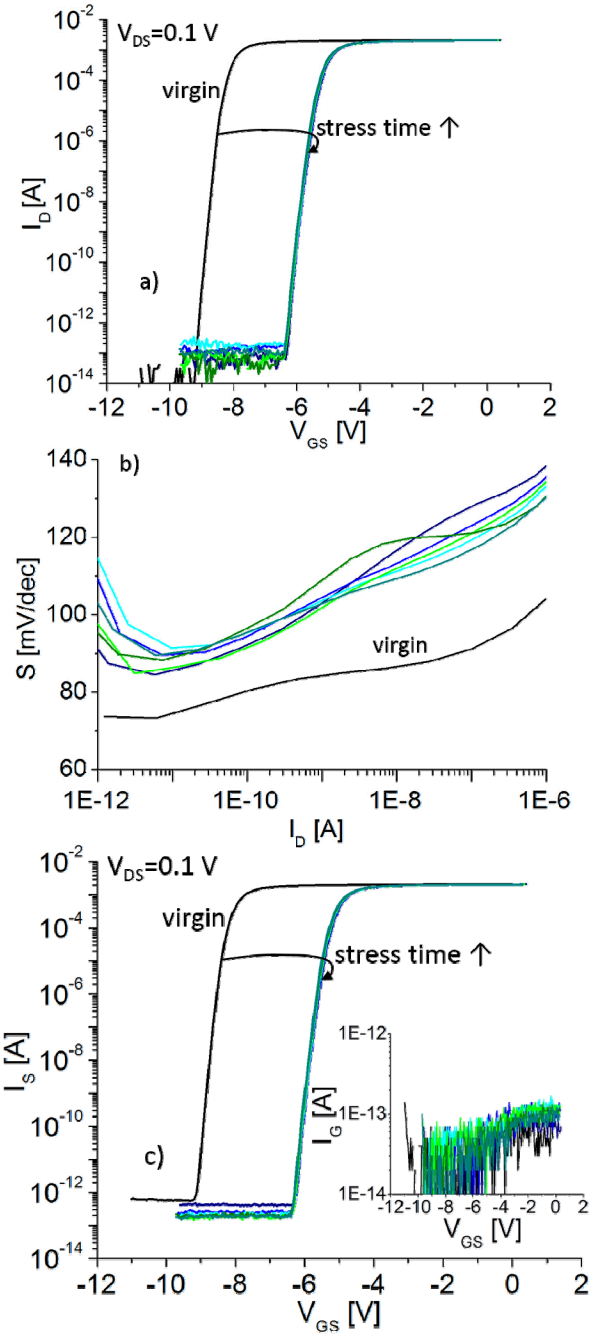

Fig. 6. a) Subthreshold I_D characteristics and b) subthreshold swing at V_{DS}=0.1 V, for a TDDB experiment at $V_{GS,stress}$=12.6 V *before* 1BD. c) Subthreshold I_S, and I_G (inset) during the same experiment. There is an initial fixed degradation of S which then stays roughly constant. I_G remains below the noise floor. I-V characterization is performed every 5 minutes.

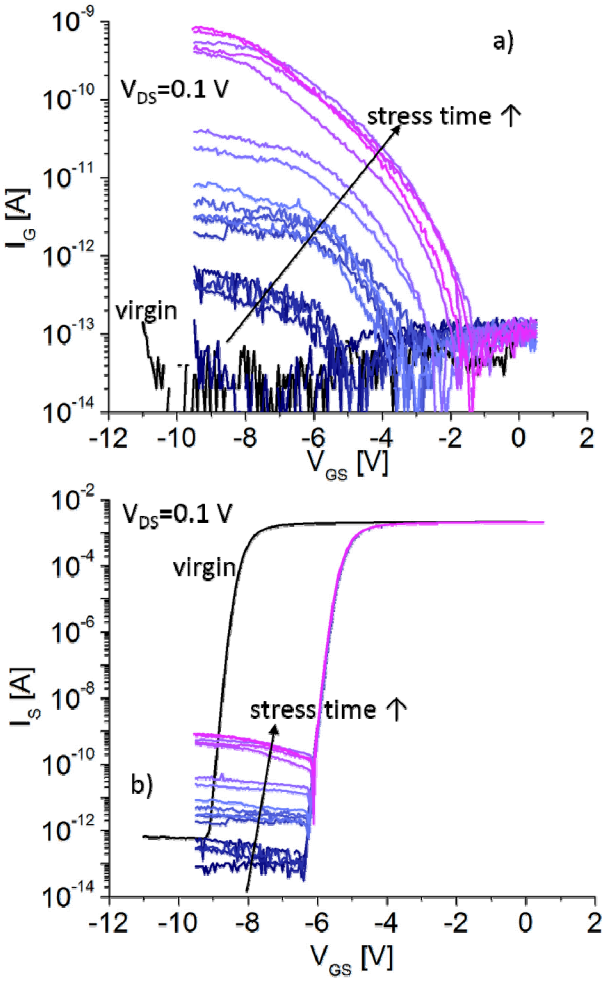

Fig. 7. a) I_G during I-V characterization every 20 s *after* 1BD ($V_{GS,stress}$=12.6 V) at V_{DS}=0.1 V. b) Subthreshold I_S during the same experiment. Leakage from the gate can be seen through the source terminal.

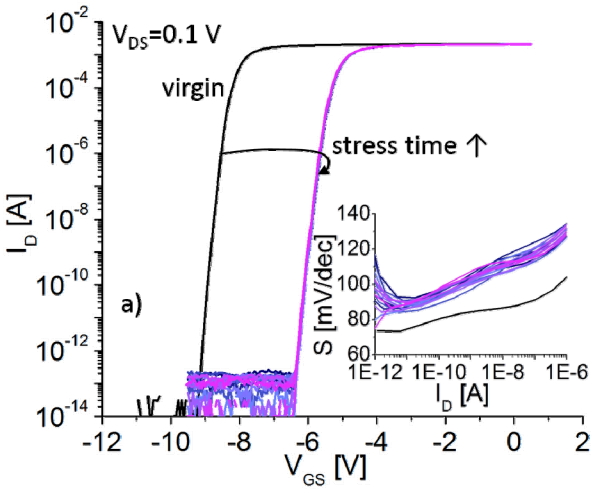

Fig. 8. Subthreshold I_D characteristics and subthreshold swing (inset) at V_{DS}=0.1 V, for a TDDB experiment at $V_{GS,stress}$=12.6 V *after* 1BD. Drain current and S remain unchanged from Fig. 5a and Fig. 5b where 1BD had not yet occurred.

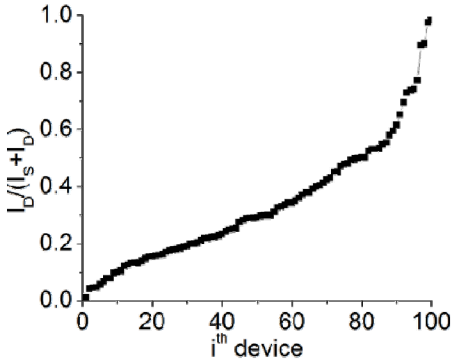

Fig. 9. Cumulative distribution plot of the ratio $I_D/(I_S+I_D)$ after HBD. V_{GS}= -0.7 V, V_{DS}=0 V for 100 devices. The higher resistance due to the longer gate-to-drain distance causes this ratio to skew more towards the source.

reveal a range of breakdown paths in some cases closer to the drain. The subthreshold swing S in the inset of Fig. 8 shows no change from that in Fig. 6b. This indicates that the mechanism responsible for the initial increase in S is unrelated to the defect generation in the dielectric that underlies breakdown.

Having seen that the gate leakage in the device pictured in Figs. 7 and 8 is closer to the source, we can follow the strategy in [22] to plot the ratio of $I_D/(I_S+I_D)$ *after* HBD as shown in Fig. 9. The ratio of the drain current to the total drain and source current (i.e. gate current) is indicative of the hard breakdown location laterally in the channel. We plot this ratio for 100 devices at V_{GS} = -0.7 V and V_{DS}=0 V. The preferential weighting towards the source that the results in Fig. 9 indicate is not unreasonable since in this device design, the gate-to-drain distance is longer than the gate-to-source distance. Therefore we expect the resistance of the drain access region $R_{Daccess}$ to be larger than that of the source access region $R_{Saccess}$.

Fig. 10 shows I_G vs. $|V_{GS}|$ for V_{GS}<0 V in a log-log scale at different temperatures after 1BD has occurred but before HBD. For smaller $|V_{GS}|$ the temperature dependence is larger,

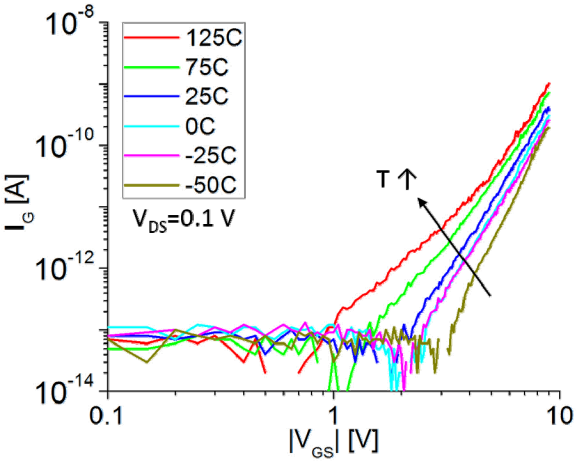

Fig. 10. Gate leakage current I_G for V_{GS}< 0 V as a function of temperature after 1BD has occurred. Temperature range is from 125ºC to -50ºC. I_G is measured at V_{DS}=0.1 V.

and it shrinks for larger $|V_{GS}|$. This behavior of the I_G temperature dependence is consistent with results in silicon

MOSFETs with SiO_2 as the gate dielectric that suggest perhaps a co-tunneling mechanism [23],[24]. I_G also shows a power law dependence. At high temperature (125°C) two exponentials in I_G are evident with slopes of 3.1 and 4.8. The slope sharpens for lower temperatures and becomes 7.7 at -50°C. These slopes are higher than reports in silicon but the overall exponential behavior is similar to what has been reported in Si MOSFETs with a SiO_2 dielectric [23]. The exponential behavior and the temperature dependence that we observe are predicted by the co-tunneling model [23].

IV. Capacitance Characterization

To gain further insight into the electrostatics of the gate stack during TDDB experiments, we have performed capacitance vs. time and capacitance vs. voltage characterization. We accomplish this by using a Capacitance Measurement Unit to simultaneously apply stress and measure gate-to-channel capacitance C_{GG}. Following this approach, we can carry out TDDB stress experiments identical to that of Fig. 1 but where we monitor the capacitance at a particular frequency instead of the gate current. In general, we do not observe (not shown) any signatures of PBD in a C_{GG} measurement, unless the measurement frequency is very low. For low enough frequency, we are able to detect 1BD due to the susceptibility of low frequency C_{GG} to bias I_G noise. This is shown in Fig. 11. In this experiment, C_{GG} is monitored at 3 kHz, and the inset of Fig. 11 shows the onset of noise indicative of 1BD. Eventually, HBD is observed at around 2460 s.

Fig. 12 shows high-frequency C-V characterization before (Fig. 12a) and after (Fig. 12b) 1BD has occurred following the same methodology in Figs. 5-8. Here, rather than measuring the subthreshold characteristics we have interrupted the TDDB stress to measure the C-V characteristics. As with the subthreshold characterization, before 1BD the device is characterized once every 5 minutes and after 1BD once every 20 s. There is a large V_T shift immediately after applying stress, most likely due to electron trapping. If we shift all of the stressed C-V curves to lie on top of the virgin sweep, as shown in Fig. 12c and Fig. 12d, we can see there is a small stretch-out of the C-V characteristics from the first stress step onward but no further change—similar to the behavior of the subthreshold degradation. No further changes were observed either before or after 1BD. This confirms that the damage to the device is minor and limited to the dielectric (most likely trapping with some interface state formation) and that the overall electrostatics of the gate stack are otherwise unaffected.

V. Discussion

Thus far, our experimentation has revealed a rich picture of dielectric breakdown in GaN MIS-HEMTs. The statistical behavior is consistent with that seen in Si devices, and the parallel distributions for time-to-first-breakdown 1BD and time to HBD strongly suggest the two have the same physical origin. Having confirmed that our stress-and-measure methodology does not affect our overall breakdown statistics, we can characterize our device in the midst of stress and explore the impact of progressive breakdown.

The subthreshold I-V characteristics show no substantial

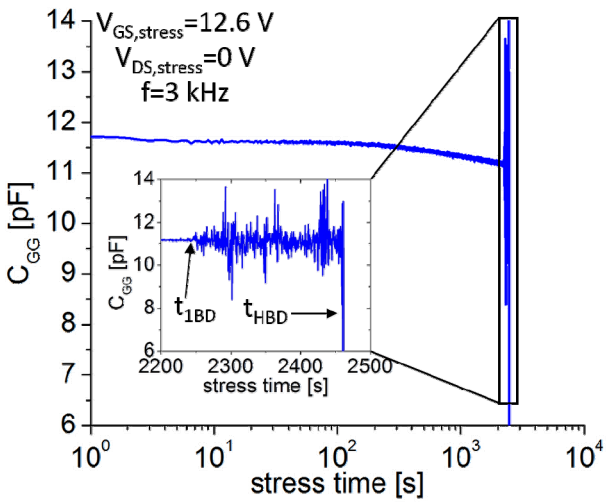

Fig. 11. Time evolution of gate capacitance at 3 kHz during a constant $V_{GS,stress}$ experiment. C_{GG} is measured at $V_{GS,stress}$=12.6 V, $V_{DS,stress}$=0 V.

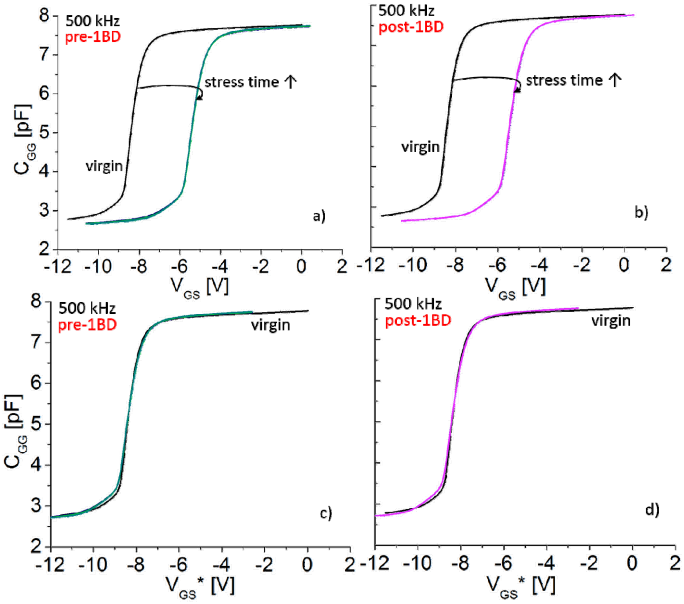

Fig. 12. C-V characteristics measured at 500 kHz and V_{DS}=0 V, a) before 1BD has occurred and b) after 1BD has occurred. No substantial change is observed in either regime. The stress C-V curves of a) and b) are shifted onto the virgin curves, shown in c) and d) respectively. C-V characterization is performed every 5 minutes before 1BD and every 20 s after 1BD.

changes before 1BD has occurred. There is small degradation in subthreshold swing S, but it shows no trend as the stress progresses. This suggests that the root cause of degradation for S is uncorrelated with the degradation in the gate dielectric. It is likely that the effect causing S degradation is also the origin of the subtle changes of the C-V characteristics after the first stress step that then remain static for the remaining duration of the TDDB stress. We do see an increase in I_G but this is only during the stress portion of our experiments and is due to SILC.

After first breakdown occurs, a much different picture emerges. The gate leakage during subthreshold characterization now begins to increase, and it does so in a step-like manner. This suggests that in this subthreshold

regime, gate leakage only increases when another defect is randomly generated during stress in or near the critical breakdown path. In parallel, SILC-related defects are continuously generated with stress throughout the dielectric area but this is not reflected in the subthreshold characterization and is likely masked by the current increase and noise emerging with the formation and growth of the percolation path. This process continues on until the percolation path becomes sufficiently conducting to release enough stored energy in the gate capacitor to cause a catastrophic event and the dielectric breaks down completely.

We also see that the leakage from the gate in the one particular device shown in this paper flows preferentially through the source terminal. However, if we examine many devices after hard breakdown we see that there is in fact a broad distribution of lateral breakdown locations in the channel, suggesting that the leakage path during PBD also may have a spread as well. This is consistent with our experimental observations (not shown here) as well as with reports in silicon MOSFETs with SiO_2 as the gate dielectric [22] and what was expected for these devices. The voltage and temperature dependence of I_G during PBD is also consistent with observed behavior in silicon.

Leveraging our ability to characterize the capacitance of our devices, we can see that the onset of 1BD does not produce noticeable damage at the AlGaN/GaN interface and further confirms that damage is limited to the gate dielectric.

In the future, we will continue to use I-V measurements and also the unique abilities of C-V measurements, such as frequency dependence, to learn more about the physics of TDDB in GaN MIS-HEMTs.

VI. Conclusions

In summary, we have developed new techniques to study TDDB in high-voltage AlGaN/GaN MIS-HEMTs, and for the first time explored progressive breakdown in these devices. The classic behavior we see is consistent with observations in silicon MOSFETs and gives hope that a lifetime model for TDDB in GaN-MISHEMTs can be developed. This requires detailed understanding of the electrostatics of the gate stack in the presence of severe trapping.

Acknowledgments

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